HARRIS SEMICONDUCTOR

# HS-6664RH

## ADVANCE INFORMATION

December 1992

**Radiation Hardened 8K x 8 CMOS PROM**

### Features

- 1.2 Micron Radiation Hardened Bulk CMOS
- Total Dose 3 x $10^6$ RAD (Si)
- Transient Output Upset >1 x $10^9$ RAD (Si)/s
- Single Event Upset < 1 x $10^{-10}$ Errors/Bit-Day
- Fast Access Time 50ns
- Single 5V Power Supply
- Single PUlse 10V Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Three-State Outputs
- NiCr Fuses
- Low Standby Current <500mA (Pre-Rad)
- Low Operating Current <30mA/MHz
- Military Temperature Range -55°C to +125°C

### Description

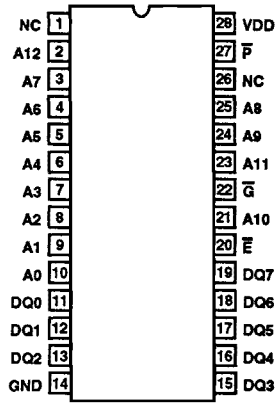
The Harris HS-6664RH is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfaceing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

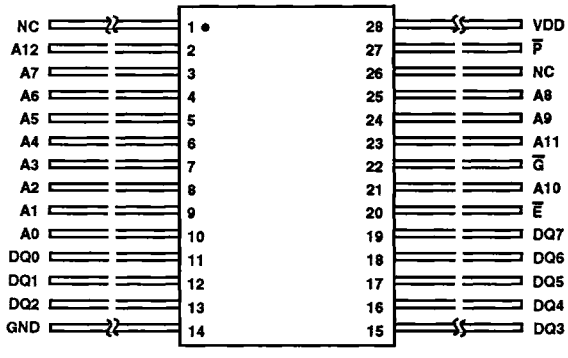
Applications for the HS-6664RH CMOS PROM include low power microprocessor based instrumentation and communcations systems, remote data acquisition and processing systems, and processor control store.

### Pinouts

28 PIN CERAMIC DIP
CASE OUTLINE D10, CONFIGURATION 3
TOP VIEW




28 PIN FLATPACK
CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW




8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.



File Number 3197

## Functional Diagram